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10/699,707	11/03/2003	Antonio F. Mondragon-Torres	TI-35731	3525

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EXAMINER	
LEE, SIU M	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com

Office Action Summary	Application No.	Applicant(s)	
	10/699,707	MONDRAGON-TORRES ET AL.	
	Examiner	Art Unit	
	SIU M. LEE	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-9,12-16,18,19,21 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-15* is/are allowed.

6)☒ Claim(s) *3-9,11,18,19 and 21* is/are rejected.

7)☒ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 3-9, 12-15, 18-19, and 21-22 have been considered but are moot in view of the new ground(s) of rejection.

With respect to the provisional double patenting rejection with the co-pending application 11/105755, since the co-pending application 11/105755 has been revived and the instant application is not in a condition of allowance, the examiner re-instate the provisional double patenting with co-pending application 11/105755.

Claim Objections

2. Claim 16 is objected to because of the following informalities:

Claim 16 recites "The method of claim 11"; claim 11 has been cancelled, the examiner suggests changing to "The method of claim 13".

Appropriate correction is required.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140

F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 5, 8, 18 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 3 and 4 of copending Application No. 11/105755. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following comparison.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim	Instant application	Claim	Co-pending application 11/105755
5	An apparatus comprising: two or more adaptive equalizers; a plurality of operational blocks that interconnect the adaptive equalizers; a first control mechanism	3 (with limitation of claims 1 and 2)	A system, comprising: a plurality of adaptive equalizers adapted to couple to a plurality of receive antennas, each of said antennas capable of receiving a multipath delay profile estimate (MDPE);

	that configures the adaptive equalizers and the plurality of operational blocks according to different signal delay profiles; a second control mechanism that disables at least one of said plurality of operational blocks according to the different signal delay profiles; and a third control mechanism that disables a computation resource of at least one of said adaptive equalizers according to the different signal delay profiles.		control logic interconnecting at least some of the adaptive equalizers; and a control mechanism that, according to different MDPEs, configures at least some of the adaptive equalizers and circuit control logic. The system of claim 1, further comprising: a second control mechanism that disables at least a portion of said control logic according to the different MDPEs. The system of claim 2, further comprising: a third control mechanism that disables a computation resource of at least one of said adaptive equalizers according to the different MDPEs.
8	An apparatus comprising:	4	A system, comprising:

	two or more adaptive equalizers; a plurality of operational blocks that interconnect the adaptive equalizers; a first control mechanism that configures the adaptive equalizers and the plurality of operational blocks according to different signal delay profiles; a second control mechanism that disables at least one of said plurality of operational blocks according to the different signal delay profiles; and a third control mechanism that disables a computation resource of at least one of said adaptive equalizers according to the different signal delay profiles, the first, second, and third control	(with limitation of claims 1-3)	a plurality of adaptive equalizers adapted to couple to a plurality of receive antennas, each of said antennas capable of receiving a multipath delay profile estimate (MDPE); control logic interconnecting at least some of the adaptive equalizers; and a control mechanism that, according to different MDPEs, configures at least some of the adaptive equalizers and circuit control logic. The system of claim 1, further comprising: a second control mechanism that disables at least a portion of said control logic according to the different MDPEs. The system of claim 2, further comprising:

	mechanisms comprise multiplexers that receive control signals according to the different signals delay profiles.		a third control mechanism that disables a computation resource of at least one of said adaptive equalizers according to the different MDPEs. The system of claim 3, wherein the first, second and third control mechanisms comprise multiplexers that receive control signals according to the different MDPEs.
18	A system comprising: two or more adaptive equalizers; a plurality of operational blocks; a means for selectively interconnecting the two or more adaptive equalizers and the plurality of operational blocks according to attributes of a signal profile; and	4	A system, comprising: a plurality of adaptive equalizers adapted to couple to a plurality of receive antennas, each of said antennas capable of receiving a multipath delay profile estimate (MDPE); control logic interconnecting at least some of the adaptive equalizers; and a control mechanism that,

	a means for disabling a computational resource of at least one of the two or more adaptive equalizers according to said attributes of the signal profile; the means for selectively interconnecting and the means for disabling comprises a plurality of multiplexers.		according to different MDPEs, configures at least some of the adaptive equalizers and circuit control logic. The system of claim 1, further comprising: a second control mechanism that disables at least a portion of said control logic according to the different MDPEs. The system of claim 2, further comprising: a third control mechanism that disables a computation resource of at least one of said adaptive equalizers according to the different MDPEs. The system of claim 3, wherein the first, second and third control mechanisms comprise multiplexers that receive control signals according

			to the different MDPEs.

(1) Regarding claims 5, 8, and 13:

From the comparison above, the only difference between the claims is the instant application recites "a plurality of operational blocks that interconnect the adaptive equalizers" while the co-pending application recites "control logic interconnecting at least some of the adaptive equalizers". Although the terms used in the instant application and the co-pending application is different, it does not define a patentably distinct invention between the two claims since they perform the same function to interconnect the plurality of adaptive equalizer.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3-8, 18-19, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda (US 5,644,597).

(1) Regarding claim 5:

Ueda discloses an apparatus (adaptive equalizer as shown in figure 14) comprising:

two or more adaptive equalizers (the adaptive equalizer in figure 14 comprises decision feedback adaptive equalizer 175 and 180 and linear adaptive equalizer 176 and 181 as shown in figure 14);

a plurality of operational blocks (square error integrating circuit 177 and 182 as shown in figure 14) that interconnect the adaptive equalizers (the square error integrating circuit 177 in interconnect between the decision feedback adaptive equalizer 175 and linear adaptive equalizer 176 and the square error integrating circuit 182 in interconnect between the decision feedback adaptive equalizer 180 and linear adaptive equalizer 181 as shown in figure 14);

a first control mechanism (delay measurement circuit 174 and 179) that configures the adaptive equalizers and the plurality of operational blocks according to different signal delay profiles (delay measurement circuit read a receive signal from receive signal memory for measuring a multi-path propagation characteristics on a channel (if the delay time of the delay wave is less than or equal to 0.35 symbol or the delay time of the delay wave is more than 0.35 symbol, column 46, line 64 – column 47, line 3) and output a control signal to select the decision feedback adaptive equalizer or the linear adaptive equalizer (column 45, lines 57-63) and configure either the decision feedback adaptive equalizer or the linear adaptive equalizer to output an equalized signal to the equalized square error integrating circuit (column 46, lines 2-6)); and

a third control mechanism that disables a computation resource of at least one of said adaptive equalizers according to the different signal delay profiles (the integrated square error value of 177 of the branch from antenna 101 in figure 14 is compare with

the integrated square error value of 177 of the branch from antenna 102 based in the delay measurement of each antenna branch and decide with branch to use, and select the branch with smaller square error and deactivate the non-selected branch with degraded, column 48, lines 34-67 and column 49, lines 44-46); (as the claim does not specified a computation resource is not included in the equalizer, the examiner interprets the computation resource is the computation resource within the equalizer as shown in figure 15, by deactivating the equalizer, the computation resource of the equalizer will also be deactivate).

Ueda fail to explicitly disclose a second control mechanism that disables at least one of said plurality of operational blocks according to the different signal delay profiles.

However, Ueda discloses deactivating one antenna branch of equalizer, it would have been obvious for Ueda to deactivate one of the square error integrating circuit of the non-selected branch because there will be no output from the decision feedback adaptive equalizer and the linear adaptive equalizer since they are deactivated. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the invention of Ueda to deactivate the error integrating circuit of the non-selected branch as taught by the instant application in order to reduce power consumption.

(2) Regarding claim 3:

Ueda further discloses that wherein each of said two or more adaptive equalizer comprises a computation resource (figure 15 shows the detail of a conventional adaptive equalizer with at least a tap coefficient update circuit (column 20, lines 40-51)).

(3) Regarding claim 4:

Ueda further discloses wherein the computation resource comprises at least one item selected from the group consisting of: a summer, a conjugate block; a multiplier, and a divider (figure 15 shows an adder 5 and multiplier in block 2).

(4) Regarding claim 6:

Ueda further discloses wherein said operational blocks comprise at least one item from the group consisting of: a signal generator, a delay line, and a summer (the examiner interpret the square error integrating circuit 177 and 182 as a signal generator for generating the integration of the squared equalized error for each antenna branch, column 46, lines 2-6).

(5) Regarding claim 7:

Ueda further disclose wherein the different signal delay profiles comprise at least one multi-path signal profile selected from the group consisting of:

sub-signals that arrive to the apparatus in consecutive chip time units;

sub-signals wherein one sub-signal comprises a substantial amount of total energy of the sub-signals;

sub-signals that do not arrive to the apparatus in consecutive chip time units;

sub-signals that arrive to the apparatus in two or more clusters (the delay time of the delay wave is less than or equal to 0.35 symbol or the delay time of the delay wave is more than 0.35 symbol, column 46, line 64 – column 47, line 3); and

sub-signals that arrive to the apparatus from more than one antenna.

(6) Regarding claim 8:

Ueda discloses an apparatus (adaptive equalizer as shown in figure 14) comprising:

two or more adaptive equalizers (the adaptive equalizer in figure 14 comprises decision feedback adaptive equalizer 175 and 180 and linear adaptive equalizer 176 and 181 as shown in figure 14);

a plurality of operational blocks (square error integrating circuit 177 and 182 as shown in figure 14) that interconnect the adaptive equalizers (the square error integrating circuit 177 in interconnect between the decision feedback adaptive equalizer 175 and linear adaptive equalizer 176 and the square error integrating circuit 182 in interconnect between the decision feedback adaptive equalizer 180 and linear adaptive equalizer 181 as shown in figure 14);

a first control mechanism (delay measurement circuit 174 and 179) that configures the adaptive equalizers and the plurality of operational blocks according to different signal delay profiles (delay measurement circuit read a receive signal from receive signal memory for measuring a multi-path propagation characteristics on a channel (if the delay time of the delay wave is less than or equal to 0.35 symbol or the delay time of the delay wave is more than 0.35 symbol, column 46, line 64 – column 47, line 3) and output a control signal to select the decision feedback adaptive equalizer or the linear adaptive equalizer (column 45, lines 57-63) and configure either the decision feedback adaptive equalizer or the linear adaptive equalizer to output an equalized signal to the equalized square error integrating circuit (column 46, lines 2-6)); and

a third control mechanism that disables a computation resource of at least one of said adaptive equalizers according to the different signal delay profiles (the integrated square error value of 177 of the branch from antenna 101 in figure 14 is compare with the integrated square error value of 177 of the branch from antenna 102 based in the delay measurement of each antenna branch and decide with branch to use, and select the branch with smaller square error and deactivate the non-selected branch with degraded, column 48, lines 34-67 and column 49, lines 44-46); (as the claim does not specified a computation resource is not included in the equalizer, the examiner interprets the computation resource is the computation resource within the equalizer as shown in figure 15, by deactivating the equalizer, the computation resource of the equalizer will also be deactivate); and the first control mechanism comprise multiplexers that receive control signal according to the different signal delay profiles (figure 17 discloses using a switch 15 to select one of a two equalizer according to a control signal from switch controller 16 as shown in figure 17; the examiner interpret a switch would provide same function as a multiplexer).

Ueda fail to explicitly disclose (a) a second control mechanism that disables at least one of said plurality of operational blocks according to the different signal delay profiles and (b) Ueda discloses deactivating according to different delay profile but fails to disclose the second and third control mechanism comprise multiplexers that receive control signals.

With respect to (a), Ueda discloses deactivating one antenna branch of equalizer, it would have been obvious for Ueda to deactivate one of the square error

integrating circuit of the non-selected branch because there will be no output from the decision feedback adaptive equalizer and the linear adaptive equalizer since they are deactivated. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the invention of Ueda to deactivate the error integrating circuit of the non-selected branch as taught by the instant application in order to reduce power consumption.

With respect to (b), it is obvious for a control mechanism for deactivating comprises multiplexer that receives control signal as teaches by Sellmair (US 6,978,405 B1) (the activation/deactivation facility consists of a multiplexer which depending on a control signal, column 7, lines 39-41).

(7) Regarding claim 18:

Ueda discloses an system (adaptive equalizer as shown in figure 14) comprising:

two or more adaptive equalizers (the adaptive equalizer in figure 14 comprises decision feedback adaptive equalizer 175 and 180 and linear adaptive equalizer 176 and 181 as shown in figure 14);

a plurality of operational blocks (square error integrating circuit 177 and 182 as shown in figure 14) that interconnect the adaptive equalizers (the square error integrating circuit 177 in interconnect between the decision feedback adaptive equalizer 175 and linear adaptive equalizer 176 and the square error integrating circuit 182 in interconnect between the decision feedback adaptive equalizer 180 and linear adaptive equalizer 181 as shown in figure 14);

a means (delay measurement circuit 174 and 179) for selectively interconnecting the two or more adaptive equalizers and the plurality of operational blocks according to attributes of a signal profile (delay measurement circuit read a receive signal from receive signal memory for measuring a multi-path propagation characteristics on a channel (if the delay time of the delay wave is less than or equal to 0.35 symbol or the delay time of the delay wave is more than 0.35 symbol, column 46, line 64 – column 47, line 3) and output a control signal to select the decision feedback adaptive equalizer or the linear adaptive equalizer (column 45, lines 57-63) and configure either the decision feedback adaptive equalizer or the linear adaptive equalizer to output an equalized signal to the equalized square error integrating circuit (column 46, lines 2-6)); and

a means for disabling a computational resource of at least one of the two or more adaptive equalizers according to said attributes of signal profile (the integrated square error value of 177 of the branch from antenna 101 in figure 14 is compare with the integrated square error value of 177 of the branch from antenna 102 based in the delay measurement of each antenna branch and decide with branch to use, and select the branch with smaller square error and deactivate the non-selected branch with degraded, column 48, lines 34-67 and column 49, lines 44-46); (as the claim does not specified a computation resource is not included in the equalizer, the examiner interprets the computation resource is the computation resource within the equalizer as shown in figure 15, by deactivating the equalizer, the computation resource of the equalizer will also be deactivate); and

the means for selectively interconnecting comprises a multiplexer (figure 17 discloses using a switch 15 to select one of a two equalizer according to a control signal from switch controller 16 as shown in figure 17; the examiner interpret a switch would provide same function as a multiplexer).

Ueda fail to explicitly disclose deactivating according to different delay profile but fails to disclose the disabling mechanism comprise multiplexers that receive control signals. However, it is obvious for a control mechanism for deactivating comprises multiplexer that receives control signal as teaches by Sellmair (US 6,978,405 B1) (the activation/deactivation facility consists of a multiplexer which depending on a control signal, column 7, lines 39-41).

(8) Regarding claim 19:

Ueda fail to explicitly disclose a means for disabling at least one of the plurality of operational blocks according to said attributes of the signal profile.

However, Ueda discloses deactivating one antenna branch of equalizer, it would have been obvious for Ueda to deactivate one of the square error integrating circuit of the non-selected branch because there will be no output from the decision feedback adaptive equalizer and the linear adaptive equalizer since they are deactivated. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the invention of Ueda to deactivate the error integrating circuit of the non-selected branch as taught by the instant application in order to reduce power consumption.

(9) Regarding claim 22:

Ueda further discloses wherein the attributes of the signal profile comprise at least one selected from the group consisting of:

a number of antennas that transmitted the multi-path signal;

a length of the multi-path signal profile (delay measurement circuit read a receive signal from receive signal memory for measuring a multi-path propagation characteristics on a channel (if the delay time of the delay wave is less than or equal to 0.35 symbol or the delay time of the delay wave is more than 0.35 symbol, column 46, line 64 – column 47, line 3));

an amount of energy in a single sub-signal of the multi-path signal;

an amount of capturable energy by a number of adaptive equalizer; and

a number of energy clusters.

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda (US 5,644,597) in view of Yang (US 6,763,074 B1)

Ueda discloses all the subject matter as discuss in claim 1 except wherein a two-stage configuration of the apparatus comprises a default mode.

However, Yang discloses wherein a two-stage configuration of the apparatus comprises a default mode (step 1600 in figure 16, the default mode is selected from a plurality of possible modes of operation, column 10, lines 17-20).

It is desirable wherein a two-stage configuration of the apparatus comprises a default mode because at least the output of a detector appears at the output of the multiplexer and if the same detector is selected, the system can continue with the pre-

selected default detector (column 1, line 65 - column 2, line 5). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Yang in the system of Ueda to provide a more efficient system.

8. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda (US 5,644,597) as applied to claim 18 above, and further in view of Juan (US 5,642,382).

Ueda discloses all the subject matter as discussed in claim 18 except the system further comprising means for sharing computational resources of the two or more adaptive equalizers.

However, Juan discloses a system that share a single set of arithmetic operators between filters of the equalizers (column 2, lines 4-10).

It is desirable to share computational resources of the two or more adaptive equalizers because it can reduce hardware requirement and lower production cost (column 2, lines 4). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Juan in the system of Ueda and Master to lower the production cost.

Allowable Subject Matter

9. Claims 12-15 are allowed.

10. Claim 16 is objected to as being dependent upon a cancelled claim.

11. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 12-15

The present invention describes a method comprising; receiving, a multi-path signal profile; determining, attributes of the multi-path signal profile, and determining attributes of the multi-path signal profile comprises determining an amount of energy in a single sub-signal of the multi-path signal profile if the length of the multi-path signal profile is less than a maximum number of taps of a single adaptive equalizer; and operating two or more adaptive equalizers, operating computational resources of the two or more adaptive equalizers, and operational blocks interconnecting said two or more adaptive equalizers according to said attributes of the multi-path signal profile. The closest prior art, Ueda (US 5,644,597) describes a similar system but fails to disclose determining attributes of the multi-path signal profile comprises determining an amount of energy in a single sub-signal of the multi-path signal profile if the length of the multi-path signal profile is less than a maximum number of taps of a single adaptive equalizer. This distinct feature has been added to independent claim 13, thus rendering claims 12-15 allowable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SIU M. LEE whose telephone number is (571)270-1083.

The examiner can normally be reached on Mon-Fri, 7:30-4:00 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Siu M Lee/
Examiner, Art Unit 2611
3/2/2009

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